**Q1.**

A student has written a computer program using an imperative high-level programming language. The program could be translated using either a compiler or an interpreter.

Describe the steps that must be completed to translate and execute the program.

Your description should include:

•   why translation is necessary

•   the differences between how a compiler and an interpreter would translate the program

•   how the machine code instructions that are used to carry out the program will be fetched and executed by the processor from main memory.

**(Total 12 marks)**

**Q2.**

The greatest common divisor of two positive integers A and B is the largest positive integer that divides both of the numbers without leaving a remainder.

For example, if A = 4 and B = 6 then:

•   4 has the divisors 1, 2 and 4

•   6 has the divisors 1, 2, 3 and 6

Therefore, the greatest common divisor of 4 and 6 is 2, since this is the biggest number which appears in the list of divisors of both 4 and 6.

The method shown in **Figure 1** is a famous method for determining the greatest common divisor of two positive integers, A and B:

**Figure 1**

****

When the procedure described in the algorithm terminates, the value in A (and also B) is the greatest common divisor of A and B.

**Figure 2 – standard AQA assembly language instruction set**

|  |  |
| --- | --- |
| LDR Rd, <memory ref> | Load the value stored in the memory location specified by <memory ref> into register d |
| STR Rd, <memory ref> | Store the value that is in register d into the memory location specified by <memory ref>. |
| ADD Rd, Rn, <operand2> | Add the value specified in <operand2> to the value in register n and store the result in register d. |
| SUB Rd, Rn, <operand2> | Subtract the value specified by <operand2> from the value in register n and store the result in register d. |
| MOV Rd, <operand2> | Copy the value specified by <operand2> into register d. |
| CMP Rn, <operand2> | Compare the value stored in register n with the value specified by <operand2>. |
| B <label> | Always branch to the instruction at position <label> in the program. |
| B<condition> <label> | Branch to the instruction at position <label> if the last comparison met the criterion specified by <condition>. Possible values for <condition> and their meanings are:EQ: equal to    NE: not equal toGT: greater than    LT: less than |
| AND Rd, Rn, <operand2> | Perform a bitwise logical AND operation between the value in register n and the value specified by <operand2> and store the result in register d. |
| ORR Rd, Rn, <operand2> | Perform a bitwise logical OR operation between the value in register n and the value specified by <operand2> and store the result in register d. |
| EOR Rd, Rn, <operand2> | Perform a bitwise logical XOR (exclusive or) operation between the value in register n and the value specified by <operand2> and store the result in register d. |
| MVN Rd, <operand2> | Perform a bitwise logical NOT operation on the value specified by <operand2> and store the result in register d. |
| LSL Rd, Rn, <operand2> | Logically shift left the value stored in register n by the number of bits specified by <operand2> and store the result in register d. |
| LSR Rd, Rn, <operand2> | Logically shift right the value stored in register n by the number of bits specified by <operand2> and store the result in register d. |
| HALT | Stops the execution of the program. |

**Labels**: A label is placed in the code by writing an identifier followed by a colon (:). To refer to a label, the identifier of the label is placed after the branch instruction.

**Interpretation of <operand2>**

<operand2> can be interpreted in two different ways, depending on whether the first character is a # or an R:

•   # – use the decimal value specified after the #, e.g. #25 means use the decimal value 25.

•   Rm – use the value stored in register m, e.g. R6 means use the value stored in register 6.

The available general purpose registers that the programmer can use are numbered 0 to 12.

Write a program **using the AQA assembly language instruction set**, shown in the **Figure 2** above, that uses the method described in **Figure 1** to calculate the greatest common divisor of two positive integers.

•   At the start, the positive integer A will be stored in memory location 102 and the positive integer B in memory location 103. Your program should use these values to find their greatest common divisor.

•   When your program terminates it should store the greatest common divisor of these two numbers in memory location 104.

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**(Total 8 marks)**

**Q3.**

Describe the principles of operation of an optical disk drive that is used to read data from an optical disk such as a CD-ROM or DVD-ROM.

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**(Total 6 marks)**

**Q4.**

USB Flash Drives (a type of SSD) are a more popular choice for transferring files such as images and word processed documents from one computer to another than CD-Rs (a type of optical disk).

Explain why this is the case.

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**(Total 1 mark)**

**Q5.**

The table below shows the standard AQA assembly language instruction set. This should be used to answer question parts **(a)** and **(b)**.

|  |  |
| --- | --- |
| LDR Rd, <memory ref> | Load the value stored in the memory location specified by <memory ref> into register d. |
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| MOV Rd, <operand2> | Copy the value specified by <operand2> into register d. |
| CMP Rn, <operand2> | Compare the value stored in register n with the value specified by <operand2>. |
| B <label> | Always branch to the instruction at position <label> in the program. |
| B<condition> <label> | Branch to the instruction at position <label> if the last comparison met the criterion specified by <condition>.Possible values for <condition> and their meanings are:         EQ: equal to               NE: not equal to         GT: greater than         LT: less than |
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•   Rm – use the value stored in register m, eg R6 means use the value stored in register 6.

The available general purpose registers that the programmer can use are numbered 0 to 12.

(a)     **Figure 1** shows an incomplete assembly language program. The intended purpose of the code is to count from 1 to 10 inclusive, writing the values to memory location 17, which is used to control a motor.

Complete the code in **Figure 1**. You may not need to use all four lines for your solution and you should not write more than one instruction per line.

**Figure 1**

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**(4)**

(b)     R1 contains the decimal value 7. What value will be contained in R1 after the instruction below is executed?

LSL R1, R1, #2

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**(1)**

**(Total 5 marks)**

**Q6.**

Explain the difference between direct addressing and immediate addressing.

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**(Total 1 mark)**

**Q7.**

A laser printer has a representation of an image stored in its memory.

Describe how it prints this image on to a piece of paper.

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**(Total 6 marks)**

**Q8.**

The following registers, listed in no particular order, are used in the Fetch-Execute cycle:

•   Current Instruction Register (CIR)

•   Memory Address Register (MAR)

•   Memory Buffer Register (MBR)

•   Program Counter (PC)

•   Status Register (SR)

Describe, **using full sentences**, the steps involved in the Fetch-Execute cycle.

Your description should cover the fetch, decode and execute stages of the cycle and should include an explanation of how the registers listed above are used.

You may use the abbreviations given above for the register names in your response, for example PC for Program Counter.

In your answer you will be assessed on your ability to use good English and to organise your answers clearly in complete sentences, using specialist vocabulary where appropriate.

**(Total 8 marks)**

**Q9.**

(a)     Explain the effect of increasing the width of the data bus.

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**(1)**

(b)     Explain precisely the effect of increasing the width of the address bus by 1 bit.

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**(1)**

**(Total 2 marks)**

**Q10.**

Explain the principles of operation of a laser printer.

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**(Total 6 marks)**

**Q11.**

(a)     Complete the table below and draw the symbol for an AND gate in the box.

|  |  |  |
| --- | --- | --- |
| Truth table for an AND gate |   | AND gate symbol |
| **Input A** | **Input B** | **Output** |
|  |   |  |
|  |   |  |
|  |   |  |
|  |   |   |

**(2)**

(b)     Using the laws of Boolean algebra, simplify the following Boolean expression.

A.B. (A + B)

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Answer \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

**(3)**

(c)     Using the laws of Boolean algebra, simplify the following Boolean expression.

(X + Y).(X + )

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Answer \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

**(3)**

**(Total 8 marks)**

**Q12.**

An integrated circuit manufacturer is looking to develop a new processor.

(a)     What would be the direct consequence on potential performance of

increasing the width of the data bus? \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

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increasing the width of the address bus? \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

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increasing the clock speed? \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

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**(3)**

(b)     A company has designed a new peripheral and is developing the I / O controller for it.

(i)      What do we mean by the term peripheral?

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**(1)**

(ii)     The I / O controller is an electronic circuit consisting of three parts. One of these parts is known as the I / O port.

What is the role of the I / O port?

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**(1)**

(iii)    Describe another part of the I / O controller.

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**(1)**

(iv)    Peripheral devices are not directly connected to the processor but make use of the system bus.

Give **two** reasons why it is **not** sensible to connect peripherals directly to the processor.

Reason 1 \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

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Reason 2 \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

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**(2)**

**(Total 8 marks)**

**Q13.**

In 1995, a high capacity hard disk drive had a storage capacity of 512 megabytes. In 2012, a typical hard disk drive of the same physical size had a capacity of 1 terabyte.

(a)     Describe the principles of operation of a hard disk drive.

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**(4)**

(b)     How many times greater is the storage capacity of a 1 terabyte hard disk drive than that of a 512 megabyte hard disk drive?

Show each stage of your working.

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**(1)**

Final answer \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

**(1)**

(c)     Give **one** development in the design of hard disk drives that has enabled this increase in storage capacity.

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**(1)**

(d)     If you are considering purchasing a high-end desktop or laptop you might be offered the option of a solid-state drive (SSD) rather than a traditional hard disk drive.

A solid-state drive is a data storage device that uses solid-state memory, similar to that in USB flash drives (memory sticks), to store data that is accessed in a similar way to a traditional hard disk drive.

Ignoring any differences in price and assuming that both drives have the same capacity, state **two** reasons why you might choose the solid-state drive.

Reason 1 \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

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Reason 2 \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

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**(2)**

**(Total 9 marks)**

**Q14.**

(a)     A machine code instruction can be split into an opcode part and an operand part.

(i)      What does an opcode represent?

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**(1)**

(ii)     What does an operand represent?

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**(1)**

(b)     State **two** advantages of writing a program in assembly language over writing a program in machine code.

Advantage 1: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

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Advantage 2: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

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**(2)**

**(Total 4 marks)**

**Q15.**

The following registers are used in the Fetch-Execute cycle:

•        Current Instruction Register (CIR)

•        Memory Address Register (MAR)

•        Memory Buffer Register (MBR)

•        Program Counter (PC)

•        Status Register (SR)

Describe, **using full sentences**, the steps involved in the Fetch-Execute cycle, making reference to how the registers above are used. Your description should cover the fetch, decode and execute phases of the cycle. You may use the abbreviations given above for the register names in your response; for example PC for Program Counter.

In your answer you will be assessed on your ability to use good English and to organise your answer clearly in complete sentences, using specialist vocabulary where appropriate.

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**(Total 6 marks)**

**Q16.**

**Figure 1** and **Figure 2** show different versions of the same program.

|  |  |
| --- | --- |
| **Figure 1** | **Figure 2** |
| **(x)               (y)                 (z)** | **(x)                (y)                        (z)** |
| 200     LOAD      7201     ADD       3202     ADD       6203     STORE     255 | 200     01010110     00000111201     11010000     00000011202     11010000     00000110203     11110000     11111111 |

(a)     What generation of programming language is shown in **Figure 1**?

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

**(1)**

(b)     In both figures above there is a column labelled **(x)**.

What would be a suitable heading for this column?

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

**(1)**

(c)     In both tables the instruction is split into two parts.

What are the names of the instruction parts in columns **(y)** and **(z)**?

**(y)** \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

**(z)** \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

**(2)**

(d)     What is the relationship between the instructions in **Figure 1** and **Figure 2**?

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**(1)**

**(Total 5 marks)**

**Q17.**

The internal components of a computer system are connected together by three buses.

(a)     State the name of the only unidirectional bus.

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**(1)**

(b)     If a computer has a 32-bit address bus, of 32 lines, it can access **4 gigabytes** of main memory for all forms of internal use.

How many additional lines does the address bus need for it to be capable of addressing up to **8 gigabytes** of main memory? Write your answer in the box below.



**(1)**

(c)     The diagram below shows how components of a computer system can be connected.



Write the correct name for each of **A, B, C** and **D** from the diagram above using only the following:

Processor, Address Bus, Data Bus, Main Memory, Keyboard and Visual Display Unit

**A** \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

**B** \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

**C** \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

**D** \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

**(4)**

**(Total 6 marks)**

**Q18.**

CD-ROM, CD-RW, Flash Memory Card and Magnetic Tape are all different types of storage media.

Complete the table below, indicating which of these storage media would be the most suitable to use in the situations described. You should not use the same medium more than once.

|  |  |
| --- | --- |
| **Situation** | **Suitable Medium** |
| Storing photographs in a compact digital camera, as they are taken |   |
| Making a backup copy of 1,000 gigabytes of data, stored on a network file server |   |
| Distributing a software package to home computer users |   |

**(Total 3 marks)**

**Q19.**

The diagram below shows the processor registers and busses that are used during the fetch part of the fetch-execute cycle, together with the main memory. The values stored in memory locations 0 to 6 in the main memory are machine code instructions.



(a)     Name the components that are labelled with the numbers 1 to 4. In the case of register names, the full names must be stated.

|  |  |
| --- | --- |
| **Number** | **Component Name** |
|  |   |
|  |   |
|  |   |
|  |   |

**(4)**

(b)     Explain what happens during the decode and execute stages of the fetch-execute cycle.

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**(3)**

(c)     The machine code instructions in the main memory in the diagram above are shown in binary.
When programmers look at machine code instructions they usually prefer to view them in hexadecimal.

State **one** reason why this is the case.

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

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**(1)**

(d)     The machine code instructions in the main memory in the diagram above were produced when an assembly language program was translated into machine code.

(i)      What type of program translator was used to do this?

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

**(1)**

(ii)     Most computer programs are initially written in an imperative high level language rather than assembly language.

Explain why this is the case.

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**(3)**

**(Total 12 marks)**

**Q20.**

The figure below shows the fetch-execute cycle. Steps 2a and 2b occur at the same time.

|  |  |
| --- | --- |
|  | **Step 1**: MAR ← [PC] **Step 2a:** PC ← [PC] + 1 **Step 2b:** MBR ← [Memory]addressed **Step 3**: CIR ← [MBR] **Step 4**: Decode Instruction **Step 5**: Execute Instruction |

(a)     State the full names of **two** of the special purpose registers that are used in the fetch part of the fetch-execute cycle.

Register 1: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

Register 2: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

**(2)**

(b)     Explain the role of the address bus, data bus and main memory during Steps 1 and 2b.

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**(2)**

(c)     Give **one** reason why Steps 2a and 2b are able to occur at the same time.

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**(1)**

**(Total 5 marks)**

**Q21.**

Peripherals can be classified as input, output or input/output (I/O) devices.

(a)     Explain what a peripheral is.

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

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**(1)**

(b)     The table below lists two peripherals.

Put **one** tick in each row to identify each peripheral as either an input, output or I/O device.

|  |  |  |  |
| --- | --- | --- | --- |
| **Peripheral** | **Input** | **Output** | **Input/Output (I/O)** |
| Mouse |   |   |   |
| Laser Printer |   |   |   |

**(2)**

**(Total 3 marks)**

**Q22.**

Radio frequency identification (RFID) is an automatic identification method. Tags attached to, or inserted into a product, an animal or a person are used to store and transmit data for remote retrieval.

A tag consists of a small chip and an antenna which enables it to receive and to respond to radio frequency signals from a reader device. Tags can be ‘read’ by supermarket shelves, microwave ovens, fork lift trucks and so on.

Each reader is typically connected to a server via a network. A server can look up the code read from the tag in a database to identify the tagged item uniquely and then take appropriate action. Tags do not need to be in line of sight to be read, and they can be read even if they are in your pocket!

Examples of the use of RFIDs include:

•        inserting a chip under the skin of a pet

•        tagging airline passengers’ luggage

•        tagging containers that are used to transport goods around the world

•        tagging euro notes

•        inserting tags inside clothes and other retail goods

(a)     Using only the applications listed above, give **two** benefits of RFIDs to organisations that might use them.

1. \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

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2. \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

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**(2)**

(b)     Using only the applications listed above, give **one** benefit of RFIDs to a member of the public.

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**(1)**

(c)     Using only the applications listed above, give **one** concern an individual might have about the use of RFIDs.

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

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**(1)**

**(Total 4 marks)**

**Q23.**



As part of the fetch-execute cycle of a computer system the processor has to fetch the next instruction. The figure above shows the main components used. They are used in the sequence 1, 2, 3, 4, 5, 6 to fetch the next instruction. Name the components by completing the table below.

|  |  |
| --- | --- |
| **Component** | **Name** |
| 1 | Program Counter |
| 2 |   |
| 3 |   |
| 4 |   |
| 5 |   |
| 6 |   |

**(Total 5 marks)**

**Q24.**

(a)     Describe what is meant by **secondary storage**.

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

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**(2)**

(b)     Which of the following is **not** a secondary storage medium?

floppy disc, flash memory, cache memory, CD-Rom

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

**(1)**

**(Total 3 marks)**

**Q25.**

The figure below shows a label from an item sold in a shop. The data from this label is captured by a computer system at the checkout.



(a)     What input device would have been used in the shop to read this label?

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

**(1)**

(b)     (i)      Give **one** advantage of having the label read by the input device given in (a) rather than having the numbers keyed in by the shop assistant.

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

**(1)**

(ii)     This type of code is used to identify items in many different situations.  State **one** advantage that it has over a character code that makes it suitable for this task.

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

**(1)**

**(Total 3 marks)**

**Q26.**

The fetch execute cycle may be described as:



(a)     Name **four** registers that are used in the Fetch Decode part of the cycle.

1. \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

2. \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

3. \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

4. \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

**(4)**

(b)     (i)      What additional steps would be required if the computer system had an interrupt mechanism?

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

**(2)**

(ii)     Where would they be placed in the above cycle?

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

**(1)**

(c)     (i)      Describe the vectored interrupt mechanism.

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

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**(3)**

(ii)     How does this mechanism make the use of interrupts more flexible?

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

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**(1)**

**(Total 11 marks)**

**Q27.**

A school plans for the school’s canteen to eliminate the need for

•        canteen staff to handle cash transactions;

•        pupils to pay with cash when purchasing meals.

Instead all payments in the canteen will be made electronically from an “electronic wallet” provided by the school to each pupil.

Pupils will be able to top up their “electronic wallet” at any time at machines located around the school which accept payment by cash, debit card and credit card.

A system designer is employed to design a system for the canteen which supports the

•        payment for meals by “electronic wallet”;

•        production of menus and price lists for display.

The designer has the following hardware in addition to computers with hard disk storage, keyboard, mouse and VDU to choose from:

Smart card reader/writer

Fingerprint scanner

Touch sensitive screen

Laser printer

Impact printer with paper roll.

(a)     For each of the above give **one** purpose of its use in this canteen system.

(i)      Smart card reader \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

**(1)**

(ii)     Fingerprint scanner \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

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**(1)**

(iii)     Laser printer \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

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**(1)**

(iv)    Impact printer \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

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**(1)**

(v)     Touch sensitive screen \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

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**(1)**

(b)     Describe the principle of operation of a touch sensitive screen.

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**(2)**

**(Total 7 marks)**

**Q28.**



(a)     The diagram above represents part of a computer system. Give the full name of **each** of the following:

(i)      ROM \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

**(1)**

(ii)     RAM \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

**(1)**

(b)     In the diagram above, what are the parts labelled (b)(i) and (b)(ii)?

(i)      \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

**(1)**

(ii)     \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

**(1)**

(c)     The system bus normally consists of three buses. Give the names of each of these **three** buses.

1. \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

2. \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

3. \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

**(3)**

(d)     What is meant by the stored program concept?

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**(2)**

(e)     Parity bits are used to ensure the accuracy of stored data.

(i)      What is meant by even parity?

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**(1)**

(ii)     Briefly describe how parity bits are used.

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

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**(2)**

**(Total 12 marks)**

**Q29.**

A football club invests in a computerised ticketing system for home matches. In addition to networked computers with hard disk storage, keyboard, mouse and VDU, the system designer of the football ticketing system has the following hardware to choose from:

Magnetic Stripe reader

Ink-jet printer

Barcode scanner

Iris scanner

Digital still camera

Smart card reader

Spectators who have pre-paid by credit card before the day of a match will only have to insert their credit card into a machine situated outside the football stadium to obtain their entrance ticket.

Other spectators will pay on the day of the match for their entrance ticket at ticket booths situated outside the football stadium or use a season ticket which is pre-purchased at the beginning of the season and used for every home match.

A season ticket holder’s ticket may be pre-loaded with electronic cash which can be spent inside the stadium on refreshments.

Spectators must present a valid ticket before being allowed into the club’s stadium.

Each spectator is allocated a numbered seat in the stadium.

The system must prevent a spectator from gaining admittance to the stadium if the spectator has been banned from the stadium.

The system must record the number of spectators inside the stadium.

The figure below shows an example of a ticket purchased on the day of a match.



Give **one** possible **use** of each hardware device in this computerised ticketing system.

(a)     Magnetic Stripe reader \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

**(1)**

(b)     Ink-jet printer \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

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**(1)**

(c)     Barcode scanner \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

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**(1)**

(d)     Iris scanner \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

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**(1)**

(e)     Digital still camera \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

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**(1)**

(f)      Smart card reader \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

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**(1)**

**(Total 6 marks)**

Mark schemes

**Q1.**

**All marks AO1 (understanding)**

**Level of response question**

|  |  |  |
| --- | --- | --- |
| **Level** | **Description** | **Mark Range** |
| 4 | A line of reasoning has been followed to produce a coherent, relevant, substantiated and logically structured response. The response covers all three areas indicated in the guidance below and in at least two of these areas there is sufficient detail to show that the student has a good level of understanding. To reach the top of this mark range, a good level of understanding must be shown of all three areas. | 10-12 |
| 3 | A line of reasoning has been followed to produce a coherent, relevant, substantiated and logically structured response which shows a good level of understanding of at least two areas indicated in the guidance below. | 7-9 |
| 2 | A limited attempt has been made to follow a line of reasoning and the response has a mostly logical structure. Either a good level of understanding of one area from the guidance has been shown or a limited understanding of two areas. | 4-6 |
| 1 | A few relevant points have been made but there is no evidence that a line of reasoning has been followed. The points may only relate to one or two of the areas from the guidance or may be made in a superficial way with little substantiation. | 1-3 |

**Guidance – Indicative Response**

**1.   Why translation is necessary**

Processor can only execute machine code instructions **A.** computer for processor

High-level instructions cannot be executed directly // high-level instructions are not machine code **A.** must be converted to machine code to be executed

**NE.** “Understand” for “execute”.

*Good level of understanding = at least one point made*

**2.   Differences between compilation and interpreting**

Compiler analyses program as a whole

Interpreter analyses program on a line-by-line basis

Compiler produces object code/executable file/machine code/bytecode

Interpreter calls subroutines within its own code to carry out commands

Compiler will not translate any of the program if it encounters an error

Interpreter translates/executes program until first error is encountered

If (unchanged) program executed twice/multiple times, compiler will only need to translate it once

Interpreter translates a program each time it is executed

Interpreter executes each line immediately after translating it

If student has written about compiler outputting bytecode then: bytecode will later be interpreted // executed by a virtual machine // just-in-time-compiled

Once translated, compiled code does not need the compiler to be present to run

An interpreter must always be present for a program that is interpreted to run

Once compiled, code will only run on one type of processor / virtual machine

Interpreter could translate the same instruction multiple times (eg if it is in a loop)

Good level of understanding = at least four points made

**3.   How machine code instructions fetched and executed**

F-E Stage 1 Fetch:

Contents of Program Counter / PC transferred to Memory Address Register / MAR

**R.** if implied the instruction is stored in the PC

Address bus used to transfer this address to main memory

Transfer of main memory content uses the data bus

Contents of addressed memory location loaded into the Memory Buffer Register / MBR

Increment (contents of) Program Counter / PC **A.** at any part of fetch process after transferring PC to MAR

Increment Program Counter / PC and fetch instruction simultaneously

Contents of MBR copied to CIR

F-E Stage 2 Decode:

Decode instruction held by the (Current) Instruction Register / (C)IR

The control unit decodes the instruction

Instruction split into opcode and operand

F-E Stage 3 Execute:

If necessary, data is fetched

If necessary, data is stored in memory

The opcode identifies the type of operation/instruction to be performed (by the processor)

Result (may be) stored in register/accumulator

The operation (identified by the opcode) is performed by the processor. **A.** ALU

Status register updated

If jump / branch required Program Counter/PC is updated

General:

Instructions will be for program (if compiled) or interpreter (if interpreted)

*Good level of understanding = at least five points made and at least two of the three stages of the F-E cycle are covered.*

**[12]**

**Q2.**

**2 marks AO2 (analysis) and 6 marks AO3 (programming)**

**Example Solution 1**

LDR R1, 102

LDR R2, 103

loop:

CMP R1, R2

BEQ finish

BGT agreaterthanb

SUB R2, R2, R1

B loop

agreaterthanb:

SUB R1, R1, R2

B loop

finish:

STR R1, 104

**Example Solution 2**

LDR R0, 102

LDR R1, 103

startloop:

CMP R0, R1

BEQ end

CMP R0, R1

BGT greater

SUB R1, R1, R0

B startloop

greater:

SUB R0, R0, R1

B startloop

end:

STR R1, 104

**Note**: Any register numbers can be used and any understandable method to identify a label.

**DPT** use of invalid register names eg R27, Rn

**6 marks AO3 (programming syntax must be correct):**

Values in memory locations 102 and 103 loaded into two different registers;

Comparison made between the values in the two registers;

If the values in the two registers are the same then the code will exit (after performing any other necessary instructions); **A.** end of program reached if not HALT instruction.

If A is greater than B then the value in the register representing B is subtracted from the value in the register representing A and result stored in register representing A;

**Note:** Award this mark even if further incorrect changes would also be made to values in registers.

If A is less than (or equal to B) / then the value in the register representing A is subtracted from the value in the register representing B and result stored in register representing B;

**Note:** Award this mark even if further incorrect changes would also be made to values in registers.

Before the algorithm exits, in all circumstance, the value in the register representing A (or the register representing B) is stored into memory location 104 (regardless of whether or not this is the gcd); A. if this is done on every iteration of a loop instead of just once.

**2 marks AO2 (concept must be understood, syntax need not be correct):**

The need for a loop has been identified and instructions are used to make the program loop back to before the comparison(s) after each subtraction has taken place;

The response provided follows the correct method to calculate the gcd of A and B, regardless of whether the syntax is correct or not, although an attempt must have been made to use the AQA instruction set;

**Max 7 if solution not fully working**

**[8]**

**Q3.**

**2 marks for AO1 (knowledge) and 4 marks for AO1 (understanding)**

|  |  |  |
| --- | --- | --- |
| **Level** | **Description** | **Mark Range** |
| 3 | A detailed, coherent, description that covers both the reading mechanism and how data is represented, demonstrating a very good level of understanding. | 5-6 |
| 2 | An adequate description, including at least three points from the list below. The description may cover one or both of the reading mechanism and how data is represented. The description is logically organised so that it makes sense when read as a whole and therefore demonstrates a reasonable understanding of the principles of operation of an optical disk drive. | 3-4 |
| 1 | A small number of relevant points have been recalled (in this case award one mark per point, up to a maximum of two from lists below). The structure of the response, or lack of it, means that only a very limited understanding of the principles of operation is demonstrated. | 1-2 |

**Indicative Content**

**Reading mechanism**

•   (Low power beam of) laser / light is shone at disk

**NE.** implication because it is reflected

•   Light is focussed on spot on track

•   (Some) light is reflected back from disk

•   Amount of light reflected back is measured // light sensor detects reflection

•   Disc spins at constant linear velocity // zoned constant linear velocity // variable (angular) velocity

**A.** variable speed

**R.** constant speed

**How data is represented**

•   Data is stored on one/spiral track

**A.** data is read in a spiral

•   Continuation of land/pit reflects light whereas transition between land and pit scatters light

**A.** land reflects light whereas pits scatter light/do not reflect light or vice-versa

**A.** “bump” for “land”

•   Transition between land and pit indicates a 1 and continuation of land / pit represents 0

**A.** land represents 1, pit 0 or vice-versa

**A.** reflection represents 1, no reflection 0 or vice-versa

**A.** “bump” for “land” or other wording which clearly reflects nature of pits and lands

**[6]**

**Q4.**

**Mark is AO1 (understanding)**

Flash drives can have a higher (storage) capacity;

**R.** references that could be to physical size eg “Flash drives are bigger”

Flash drives have faster access / read / write times;

No drive is required to use a flash drive // flash drive and medium are integrated;

Flash drives can be reused;

Flash drives are more compact;

Flash drives not damaged by scratches;

**NE.** more robust without a reason why

**R.** points about cost unless they are supported by a reason, such as no separate drive being required

**NE.** more portable unless this is supported with a valid reason that would not also apply to a CD

**[1]**

**Q5.**

(a)  **Marks are for AO3 (program)**

**Answer 1**

1. ADD R0, R0, #1 ;

2. CMP R0, #11 ;

3. BNE; startloop ;

**Answer 2**

1. ADD R0, R0, #1 ;

2. CMP R0, #11 ;

3. BEQ endloop ;

4. B startloop ;

**Answer 3**

1. CMP R0, #10 ;

2. BEQ endloop ;

3. ADD R0, R0, #1 ;

4. B startloop ;

**Answer 4**

1. ADD R0, R0, #1 ;

2. CMP R0, #11 ;

3. BLT; startloop ;

**Stop marking when the first incorrect command is encountered. Mark response against whichever alternative gives the highest mark.**

**I**. Any extra commands which do not effect operation of program.

**4**

(b)  **Mark is for AO2 (apply)**

2810 // (000)111002;

**TO**. If two answers given and one is incorrect.

**I**. Lack of subscript.

**1**

**[5]**

**Q6.**

**Mark is for AO1 (understanding)**

Direct addressing means that the operand is the (memory) address/register number (of the datum) whereas immediate addressing means the operand is the datum ;

**Note:** Must be clear that the operand is being used.

**[1]**

**Q7.**

**2 marks for AO1 (knowledge) and 4 marks for AO1 (understanding)**

**Level of response question**

|  |  |  |
| --- | --- | --- |
| **Level** | **Description** | **Mark Range** |
| 3 | At least five points have been made showing knowledge of five steps in the process. The description shows a thorough level of understanding and all of the steps have been correctly sequenced. | 5-6 |
| 2 | At least three points have been made showing knowledge of three steps in the process. Good, mostly correct understanding of the process is demonstrated between 3 or more steps. | 3-4 |
| 1 | At least one point has been made showing knowledge of one step in the process. Some understanding may be shown if two steps are covered and correctly sequenced. | 1-2 |

**Points may include:**

Print drum coated in (positive static) charge

Printer generates bitmap of page from the data

Laser beams shone / directed at / draws on print drum

Via rotating (octagonal) mirror

Laser is modulated (turned on & off)

Laser removes / neutralises / reverses electric charge on drum

where image should be dark / black

Toner is given (positive) charge

Charged drum picks up toner

For drum/laser mechanisms, one for each colour (cyan etc)

Toner transferred (from drum) to paper / paper rolled over drum (to transfer toner)

Toner is fused / bonded / melted / stuck to paper (by heated rollers / pressure) (must be clear that toner is already on paper when it is fused, not still on drum)

**A**. Reversal or lack of polarity of static charge.

**[6]**

**Q8.**

**Key points of subject criteria:**

FETCH:

Contents of Program Counter/PC transferred to Memory Address

Register/MAR;

Address bus used to transfer this address to main memory;

Contents of addressed memory location loaded into the Memory Buffer Register/MBR;

Transfer of content uses the data bus;

Increment contents of Program Counter/PC;

Increment Program Counter/PC and fetch simultaneously;

Transfer content of Memory Buffer Register/MBR to the Current Instruction Register/CIR;

**A**. Increment PC at any part of fetch process after transfer to MBR

**A**. Reference to MDR (memory data register) instead of MAR

DECODE:

Decode instruction held by the Current Instruction Register/CIR;

The control unit decodes the instruction;

Instruction split into opcode and operand(s);

EXECUTE:

If necessary, data is fetched;

The opcode identifies the operation to be carried out by the processor;

Execute instruction by relevant part of processor;

Result stored in accumulator/ (destination) register;

Status Register (SR) updated;

If jump/branch instruction Program Counter/PC is updated;

|  |
| --- |
| **Mark Bands and Description** |
| 7-8 | *To achieve a mark in this band, candidates must meet the subject criterion (SUB) and all 5 of the quality of written communication criteria (QWCx).* |
| *SUB* | Candidate has provided at least 7 points. At least one point made for each of the fetch, decode and execute stages. Answer must mention at least 3 registers. |
| *QWC1* | Text is legible. |
| *QWC2* | There are few, if any, errors of spelling, punctuation and grammar. Meaning is clear. |
| *QWC3* | The candidate has selected and used a form and style of writing appropriate to the purpose and has expressed ideas clearly and fluently. |
| *QWC4* | Sentences (and paragraphs) follow on from one another clearly and coherently. |
| *QWC5* | Appropriate specialist vocabulary has been used. |
| 4-6 | *To achieve a mark in this band, candidates must meet the subject criterion (SUB) and 4 of the 5 quality of written communication criteria (QWCx).* |
| *SUB* | Candidate has provided at least 4 points covering at least 2 of the fetch, decode, execute stages. Answer must mention at least 2 registers. |
| *QWC1* | Text is legible. |
| *QWC2* | There may be occasional errors of spelling, punctuation and grammar. Meaning is clear. |
| *QWC3* | The candidate has, in the main, used a form and style of writing appropriate to the purpose, with occasional lapses. The candidate has expressed ideas clearly and reasonably fluently. |
| *QWC4* | The candidate has used well-linked sentences (and paragraphs). |
| *QWC5* | Appropriate specialist vocabulary has been used. |
| 1-3 | *To achieve a mark in this band, candidates must meet the subject criterion (SUB) and 3 of the 5 quality of written communication criteria (QWCx).* |
| *SUB* | Candidate has made a small number of relevant points. |
| *QWC1* | Most of the text is legible. |
| *QWC2* | There may be some errors of spelling, punctuation and grammar but it should still be possible to understand most of the response. |
| *QWC3* | The candidate has used a form and style of writing which has many deficiencies. Ideas are not always clearly expressed. |
| *QWC4* | Sentences (and paragraphs) may not always be well-connected. |
| *QWC5* | Specialist vocabulary has been used inappropriately or not at all. |
| 0 | Candidate has made no relevant points. |

**[8]**

**Q9.**

(a)  Effective speed at which data can be retrieved will be increased;

**A**. Larger “chunks” of data/instruction can be fetched in one operation

**Max 1**

(b)  The amount of available memory locations / addressable locations will double;

**NE**. increases amount of memory

**1**

**[2]**

**Q10.**

Page printer;

Print drum coated in (negative static) charge;

Printer generates bit map of page;

Laser beams shone/directed at/"draws" on print drum;

Via rotating (octagonal) mirror;

Laser is modulated (turned on & off);

Laser removes/neutralises/reverses electric charge on drum; where image should be dark/black;

Toner is given (negative) charge;

Charged drum picks up toner;

Toner transferred from drum to paper; ("from drum" may be implicit in order of answer)

Toner is fused/bonded/melted/stuck to paper by (heated rollers/pressure); (must be clear that toner is already on paper when it is fused, not still on drum)

**I**. incorrect charges e.g. positive when should be negative

**Max 6**

**[6]**

**Q11.**

(a)     **Marks are for AO1 (knowledge)**

|  |  |  |  |
| --- | --- | --- | --- |
| **A** | **B** | **Q** |  |
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

**1 mark:** Table completed correctly;

**1 mark:** AND gate symbol drawn;

**2**

(b)     **Marks are for AO2 (apply)**

A.B.(A + B)

A.B.A + A.B.B ; [expansion of brackets]

B.A + A.B ;        [use of A.A = A]

A.B ;                  [use of A + A = A]

**1 mark:** Final answer: A.B;

**Max 2 for working**

**3**

(c)     (**Marks are for AO2 (apply)**

X + Y).(X + NOT Y)

XX + X(NOT Y) + XY + Y(NOT Y) ; [expansion of brackets]

X + X(NOT Y) + XY ; [use of X.X = X or use of Y(NOT Y) = 0 ]

X ( 1 + NOT Y + Y ) ; [use of 1 + X = 1]

**1 mark:** Final answer - X;

**Max 2 for working**

**3**

**[8]**

**Q12.**

(a)     increase the number of bits that can be transferred at one time ;

**A** increase rate of data transfer;

increases the number of (memory) addresses / addressable locations / /

increase the maximum amount of primary store / memory (possible);

instructions performed more quickly / / instructions executed at faster rate / /

fetch execute cycle will happen faster / /
increased heat may cause malfunctioning of device / / overheating;

**A** calculations / operations / commands for instructions

**3**

(b)     (i)      a (hardware) device / component that is not part of the CPU;

**NE** processor / computer

a (hardware) device not directly under the control of the processor / CPU;

a device that communicates through an I / O controller;

external hardware / device;

**R** examples alone

**MAX 1**

(ii)     to allow exchange of data / instructions / signals between the processor and the peripheral;

**A** communicate

**R** information

**NE** To allow the device to be connected

**1**

(iii)    Electronics that interface the controller to the system bus;

Electronics appropriate for sending signals to the device connected to the computer;

**MAX 1**

(iv)    Each peripheral operates in a different way;

Not sensible to design a processor to control every possible peripheral;

A new type of peripheral would require the processor to be redesigned;

Peripherals may operate at a different voltage from the processor;

Peripherals will usually operate at a slower rate than the processor (requiring buffering);

**MAX 2**

**[8]**

**Q13.**

(a)     Magnetic (medium);
Binary digits / bits / 0s and 1s / data represented by magnetising spots on disk // changing magnetic properties of disk;
Disk made up of platter(s);
Disk divided into tracks and sectors;
**A** either tracks or sectors alone
Tracks are concentric circles // organised into cylinders
Drive head can move in / out // moves to track / cylinder // moves radially;
Disk continuously spinning (while in operation);
Disk spins at high speed // feasible example of speed;
Data read / written as correct sector passes under read / write head;
**A** drive head
Data transferred in sectors / blocks;
Medium and drive / device in sealed enclosure;
Hard disk drive is a random access device;
**A** Head parked / not over disk when not in use // head must not touch surface when in use;
**A** Use of cache / buffer to speed up data transfer;

**Max 3** if candidate talks about lasers / making holes / pins / engraving

**Max 4**

(b)     512 MB x 2 = 1024 MB = 1GB
1GB x 1024 = 1 TB

2 x 1024 = 2048

Award mark for a clear movement between MB – GB - TB making use of 1024 ;

Final answer: 2048;

**Acceptable alternative** (as many hard drive manufacturers do not use the 1024 principle) :

1 TB = 1000 GB = 1000000 MB;

1000 000 / 512 = 1953.125;
(mark to be awarded for understanding the calculation needed)

Final answer : 1953.125;

**A**  Accept a final answer that has involved some approximation as a no calculator paper.(2000;)

**Alternative**

240 / 229 ; = 211;

**Max 2**

(c)     More platters (which are packed closer);
Greater density of data on each platter;
More tracks on a platter // more cylinders;
Change to perpendicular magnetic domains;
Ability to write smaller magnetic domains/parts // smaller read / write heads;
Use of different alloy materials for the platters;

**Max 1**

(d)     Faster access speed // faster booting of operating system //
faster data transfer / read / write speeds;
Silent operation;
Are lighter;
Less heat generated;
Less power required // longer battery life;
Less susceptible to damage from physical shocks //
more robust (due to no moving parts);

**A** quicker as no need to wait for read / write head to move // sector to be underneath read / write head;

**NE** quicker (without explanation)
**NE** better performance (without explanation)

**Max 2**

**[9]**

**Q14.**

(a)     (i)      Indicates the basic machine operation / function / command;
Executable binary code;
**A** “instruction” – with a valid example

**Max 1**

(ii)     Represents a single item of (binary) data / a single value;
Represents a memory address / storage location;
The value that the instruction operates on;

**A** parameter for the operation
**NE** “address”

**Max 1**

(b)     Easier to understand;
Takes less time to code (as using mnemonic opcodes and hex operands);
Fewer mistakes made in coding;
Ability to add comments to code;
Use of symbolic names for operands // easier to remember opcodes / mnemonics;
Use of labels;
Easier to maintain / debug;

**NE** easier to read / code / write
**NE** quicker
**A** converse points if clearly discussing machine code

**Max 2**

**[4]**

**Q15.**

Key points of subject criteria:

**Fetch:**Contents of Program Counter / PC transferred to Memory Address Register / MAR;
Address bus used to transfer this address to main memory;
Contents of addressed memory location loaded into the Memory Buffer Register / MBR;
Transfer of content uses the data bus;
Increment contents of Program Counter / PC;
Increment Program Counter / PC and fetch simultaneously; **A** any part of fetch process
Transfer content of Memory Buffer
Register / MBR to the Current Instruction
Register / CIR

**Decode:**
Decode instruction held by the Current
Instruction Register / CIR;
The control unit decodes the instruction;
Instruction split into opcode and operand;

**Execute:**If necessary, data is fetched;
The opcode identifies the type of instruction it is;
Execute instruction by relevant part of processor;
Result stored in accumulator;
Status register updated;
If jump / branch instruction Program Counter/PC is updated;

*To achieve a mark in this band, a candidate must meet the subject criterion (SUB) and 4 of the 5 quality of language criteria (QLx).*

|  |  |
| --- | --- |
| *SUB*  | Candidate has provided at least 6 points. At least one point made for each of the fetch, decode and execute stages. Answer must mention at least 3 registers. |
| *QL1* | Text is legible. |
| *QL2* | There are few, if any, errors of spelling, punctuation and grammar. Meaning is clear. |
| *QL3* | The candidate has selected and used a form and style of writing appropriate to the purpose and has expressed ideas clearly and fluently. |
| *QL4* | Sentences and paragraphs follow on from one another clearly and coherently. |
| *QL5* | Appropriate specialist vocabulary has been used. |

**6**

*To achieve a mark in this band, candidates must meet the subject criterion (SUB) and 4 of the 5 quality of language criteria (QLx).*

|  |  |
| --- | --- |
| *SUB*  | Candidate has provided at least 4 points covering at least 2 of the fetch, decode, execute stages. Answer must mention at least 2 registers |
| *QL1* | Text is legible. |
| *QL2* | There may be occasional errors of spelling, punctuation and grammar. Meaning is clear. |
| *QL3* | The candidate has, in the main, used a form and style of writing appropriate to the purpose, with occasional lapses. The candidate has expressed ideas clearly and reasonably fluently. |
| *QL4* | The candidate has used well-linked sentences and paragraphs. |
| *QL5* | Appropriate specialist vocabulary has been used. |

**4–5**

*To achieve a mark in this band, candidates must meet the subject criterion (SUB). The quality of language should be typified by the QLx statements.*

|  |  |
| --- | --- |
| *SUB* | Candidate has provided at least one valid point. |
| *QL1* | Most of the text is legible. |
| *QL2* | There may be some errors of spelling, punctuation and grammar but it should still be possible to understand most of the response. |
| *QL3* | The candidate has used a form and style of writing which has many deficiencies. Ideas are not always clearly expressed. |
| *QL4* | Sentences and paragraphs may not always be well-connected or bullet points may have been used. |
| *QL5*  | Specialist vocabulary has been used inappropriately or not at all. |

**1–3**

Candidate has not made reference to any of the points above.

**0**

**[6]**

**Q16.**

(a)     Second (generation);
**A** 2
**R** assembly code / language

*Note: Adding “assembly” / “assembler” does not talk out a valid mark for second / 2*

**1**

(b)     (memory) Address / location / offset;
**A** line number
**R** instruction number

**1**

(c)     (y) Opcode / operation code;
**A** op-code
**NE** operation
(z) Operand;

**2**

(d)     **Individual Instructions:**One to one / each assembly language instruction translates to one machine code instruction;

**Programs:**Figure 1 assembly language equivalent of figure 2 // figure 2 machine code version of figure 1 // figure 2 is assembled version of figure 1;
**NE** figure 2 “binary version” of figure 1
**NE** different generations of language

**1**

**[5]**

**Q17.**

(a)     Address (bus);

**1**

(b)     1;
**R** 33

**1**

(c)     A – Visual display unit;     **A** VDU
B – Processor;                **R** CPU
C – (Main) memory;
D – Keyboard;

**4**

**[6]**

**Q18.**

(a)     Flash Memory (Card);
**R** memory card

**1**

(b)     Magnetic Tape;

**1**

(c)     CD-ROM;
CD-RW;
**A** Flash Memory Card if not given in first question part

**1**

**[3]**

**Q19.**

|  |  |
| --- | --- |
| (a)     **Number** | **Component Name** |
| 1 | Memory Address Register |
| 2 | Address Bus |
| 3 | Memory Data / Buffer Register |
| 4 | Data Bus |

**4**

(b)     The instruction is held in the CIR;
**A** IR
The control unit / instruction decoder decodes the instruction;
The opcode identifies the type of instruction it is;
Relevant part of CPU / processor executes instruction;
**A** ALU
Further memory fetches / saves carried out if required;
Result of computation stored in accumulator / register / written to main memory;
Status register updated;
If jump / branch instruction, PC is updated;
**A** SCR

**Max 3**

(c)     Can be displayed in less space;
**R** takes up less space **NE**Easier to remember / learn / read / understand;
Less error prone;

**Max 1**

(d)     (i)     Assembler;

**1**

(ii)     HLLs are problem oriented;
HLL programs are portable // machine / platform independent ;
English like **keywords / commands/ syntax / code**;
**R** closer to English
Less code required // less tedious to program //
one to many mapping of HLL statements to machine code commands;
Quicker/easier to understand / write / debug /learn / maintain code;
**R** just quicker/easier
HLLs offer extra features e.g. data types / structures // structured statements // local variables // parameters // named variables/constants;
**R** procedures / modular
**A** example of a data structure
**NE** “extra features” without example
Speed of execution not crucial for most tasks so faster execution of assembly language not required;
Most computer systems have a lot of (main) memory / RAM so compact object code not essential;
**A** converse points for Assembly Language

**3**

**[12]**

**Q20.**

(a)     Program Counter;
**A** Sequence Control Register
**R** Next Instruction
Register
Current Instruction Register;
**A** Instruction Register
Memory Buffer Register;
**A** Memory Data Register
Memory Address Register;

**Max 2**

(b)     Address in MAR/address to fetch instruction from, sent down Address
Bus to Main Memory;
**R** address in PC (program counter)
Contents of address accessed in Main Memory;
**A** by implication if
contents of address location referred to during data transfer
Contents of address location//instruction//data passed down Data Bus
into MBR/to processor;
**A** MDR instead of MBR
**A** RAM for Main Memory

**Max 2**

(c)     Order of execution unimportant/one step does not rely on prior completion of the other;
Steps carried out by different (hardware) devices/components;
**A** operations are independent
**A** operations use different registers
**R** using different buses

**Max 1**

**[5]**

**Q21.**

(a)     A (hardware) device that is not part of the CPU;
An external (hardware) device;
**A** Not built into / part of (main) computer (system) // Outside computer
**R** Can be connected to / attached to / plugs into a computer
**R** Examples alone
**R** Component for device
**R** Processor for CPU

**1**

(b)

|  |  |  |  |
| --- | --- | --- | --- |
| **Peripheral** | **Input** | **Output** | **Input/Output (I/O)** |
| Mouse | ✔ |   |   |
| Laser Printer |   | ✔ |   |

*1 mark for each correctly placed tick***R** Answers with more than one tick on a row.

**2**

**[3]**

**Q22.**

(a)     **RFID**

Cut down on theft;

**A** prevent (Bod)

Cut down on money laundering;

Cut down on lost items/ can identify found items;

Ability to track goods being sent around the world;

Keep supermarket shelves stocked;

Easier for fork lift trucks to find the correct item in a warehouse;

Know customers’ purchasing habits;

*1 mark for each of 2 benefits to max*

**2**

(b)     If your pet is lost / stolen, it can be identified;

Less chance of your baggage going astray;

Lost items more easily retrieved / found;

*benefit*

**1**

(c)     Loss of privacy / can be tracked wherever you go;

Powers that be’ know where you spend your money;

*1 concern*

**1**

**[4]**

**Q23.**

|  |  |
| --- | --- |
| Component | Name |
| 1 | Program Counter |
| 2 | Memory Address Register; **A** MAR |
| 3 | Address Bus; |
| 4 | Data Bus; |
| 5 | Memory Data Register/ Memory Buffer Register;       **A** MDR/MBR |
| 6 | Current Instruction Register; A Instruction Register/IR/CIR |

**[5]**

**Q24.**

(a)     A non-volatile / stores a permanent copy / not lost when computer switched off; storage medium; that is not directly accessible to the processor / outside main memory;

**2**

(b)     Cache memory

**1**

**[3]**

**Q25.**

(a)     Barcode reader / wand / scanner;

*If 2 answers given – TO*

**1**

(b)     (i)      Less chance of error / greater accuracy; BOD ‘No Error’// scanning by device faster;

**A** Quicker (allow in this case)

**R** harder to forge

**1**

(ii)     The bars can be read up-side-down/ has vertical symmetry;

A can be read even if not in perfect condition;

**1**

**[3]**

**Q26.**

(a)     Program Counter; Sequence Control Register/Instruction Pointer

Instruction Register// Current Instruction Register;

Memory Buffer Register// Memory Data Register;

Memory Address Register;

Penalise initials once only

**4**

(b)     (i)      Test for an interrupt/ check priority of interrupt

Identify the source of the interrupt;

Save and/or restore the volatile environment/registers;

Service the interrupt; A handle the interrupt

Disable (lower priority) interrupts

*Max 2*

**2**

(ii)     Placed between Execute and Fetch;

**A** before Fetch/ after execute R at end of cycle

**1**

(c)     (i)      Interrupting device/ source supplies;

An offset/vector;

**A** index/indexed address added to the base address;

**A** base register

Gives the start address of interrupt service routine/ ISR//

Address vector table cell contains start address of ISR/

**R** Interrupting device supplies start address of ISR

**3**

(ii)     A different routine can be easily introduced//routine can be relocated/ dynamically loaded; *or words to this effect*

**A** The interrupting device only needs to supply a new offset

**1**

**[11]**

**Q27.**

(a)     (i)      To read (or synonym)\_amount of electronic cash (or synonym) stored on card/to alter (or synonym, e.g. store/topup) the amount of cash (or synonym) stored on card **A** To read debit/credit card to top up the wallet (mush have both point R. to read card);

**A** Credit / Balance / Money / Value instead of cash

*Focus is canteen*

**1**

(ii)     To identify a pupil//to check smart card belongs to pupil//to identify staff//for staff to login;

**A** Converse
**R** For security reasons

**1**

(iii)     To print a menu/price list.

*Required by specification*

**R** Produce menu/ price list
**R** print summaries/stock lists

**1**

(iv)    To **print** receipts

**R** Produce receipts
**R.** Print invoice
**A** To print end of day summaries;

**1**

(v)     For canteen staff to enter transaction into computer system or equivalent

**R** when using cash machines
**A** For pupils to look up menu/prices//staff to create menu/change prices

**1**

(b)     Either marks awarded for (i) The technique (ii) Position detection (iii) Action

Region immediately in front of screen monitored//Beams of infra-red light projected across screen//other methods, e.g. capacitive membrane;

Position of e.g. finger determined (detected)//beam broken at a certain position;

Position matched to an action performed by computer;

R. Heat sensitive technique

*Max 2*

***OR***

***A*** *A screen which allows users to make choices by touching areas of screen;*

*Max 1*

***2***

***[7]***

**Q28.**

(a)     (i)      Read Only Memory;

**1**

(ii)     Random Access Memory;

**1**

(b)     (i)      Disk Controller;

**1**

(ii)     Network Interface Card//Network Adapter;

**A** Network Card

**1**

(c)     Address Bus;

Control Bus;

Data Bus;

**3**

(d)     Program stored in main memory;

**A** RAM/IAS

**R** ROM

Instructions fetched and executed by processor *(concept)*;

**A** CPU

Can be replaced by another program;

**R** cache

**2**

(e)     (i)      The number of 1s (including the parity bit) comes to an even number;

**1**

(ii)     Used to check for errors when data is read / transferred;

Parity bit regenerated / recalculated;

Compared with parity bit;

*Any 2*

**2**

**[12]**

**Q29.**

(a)     Reading credit card details;

**R** Debit card

**1**

(b)     Printing tickets // printing spectator statistics;

**1**

(c)     Reading barcode (on ticket)//scanning/reading ticket for ticket details // scanning/ reading ticket (barcode) to allow entrance // scanning/reading ticket to check ticket is valid;

**R** Scanning ticket // scanning barcode

**A** Scanning ticket...some phrase implying ticket details obtained

**R** Reading ticket on its own

**1**

(d)     NB Must be spectator

**Identifying** banned spectator (by iris pattern) // checking ticket holder is ticket purchaser // Photographing spectator to be banned;

**1**

(e)     NB Must be spectator

Photographing spectator for identification (by facial pattern recognition) // checking ticket holder is ticket purchaser // checking season ticket holder is genuine;

**R**. Photographing spectator on its own

**1**

(f)      Reading details from season ticket holder smart card; Reading credit card details;

**1**

**[6]**